



The CM5160 MDDI-to- Interface Converter and Bridge Display Controller for Wireless Handsets

**Bridging the Serial Display Standards Gap for Reduced
Manufacturing Costs**

White Paper

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The Evolution of Standardized Display Interfaces

Display technology utilized by mobile handsets has undergone a dramatic change in the last several years. The evolution from simple liquid crystal displays (LCDs) to full color VGA resolution displays has enabled the high-end mobile handset to become a hybrid between a personal digital assistant, digital camera, personal media player, and internet appliance. These feature-packed, all-in-one handsets often employ thin film transistor (TFT) LCDs with resolutions up to wide format VGA displays with 24 bit per pixel color depths.

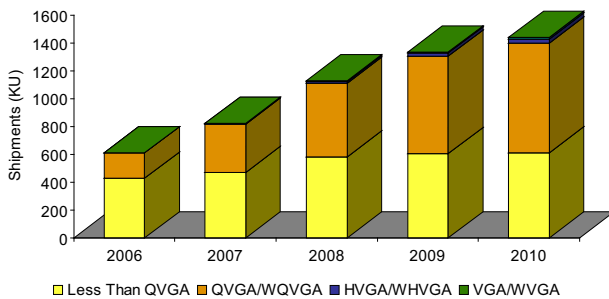


Figure 1. TFT LCD Demand (Source: iSuppli 11/2007)

Traditional Parallel Display Interfaces

These new requirements have created challenges for handset designers, especially from an electromechanical perspective. Many of today's handsets are of the clamshell, sliding mount or cycloidal variety, establishing the need for a reliable mechanical and electrical interface between two physically attached modules. The display is typically in one section of the handset while the host processor is in the other. The electrical connection is made through a parallel interface via a flex cable passing through the mechanical interface.

While this approach has worked fine for low resolution display interfaces, today's higher resolution displays require a minimum of a 24-bit data bus and 4 control signals. As a result, power management, electromagnetic interference (EMI) and flex cable reliability have rapidly become challenging design issues for designers seeking to remain with these wide, parallel interfaces. Handset designers are looking for innovative solutions for high resolution handset display interfaces that can address these design issues.

The Move to Serial Display Interfaces

Many designers have opted to utilize a serial, low voltage differential signaling (LVDS) display interface. Using data packets to transport the display information from the host CPU to the display, the serial display interface can be utilized with as few as 4 signal lines. Increases in display resolution are accommodated by increasing the packet data rate, which is easily

achieved with a small number of high-speed, low-level differential signal lines that make up the interface. While it is more complex to design from a logic standpoint, the simplicity of the serial display interface has resulted in a number of benefits including significantly lower EMI emissions, lower power consumption, higher mechanical reliability and a more easily scalable architecture.

As design interest grew, a number of serial interface solutions emerged. Chipmakers created their own proprietary serial interfaces with the hopes that their serial solution would gain market acceptance. While a step in the right direction, these proprietary solutions, comprised of a discrete transmitter or host and a discrete receiver or client, required too much board space and, with their additional expense, put too much additional burden on already tight handset bill-of-materials (BOMs).

Industry Standards Emerge

Standardization of a serial interface specification for handset displays would permit the integration of the host function into the mobile handset CPU and the client function into LCD display controller, thereby reducing the board space and cost requirements. Unfortunately, the efforts at industry standardization of a serial interface split between two camps. The first standard to achieve a level of industry acceptance was the Mobile Display Digital Interface (MDDI) standard, endorsed by QUALCOMM and ratified by the Video Electronics Standards Association (VESA). QUALCOMM has integrated MDDI based hosts into many of their CDMA and WCDMA CPUs for advanced handsets. Handsets featuring the MDDI interface began to appear in 2007.

A second standard was developed by an industry consortium called the Mobile Industry Processor Interface (MIPI™) Alliance. The MIPI™ Alliance DSI standard was ratified in 2008 and has been endorsed by many leading mobile CPU providers with solutions based upon GSM and WCDMA air standards. Handsets featuring the MIPI™ DSI serial interface standard are expected to be available by early 2009.

To address broad market requirements, major handset OEMs use CPUs from multiple companies to address different radio standards, features and price and performance points. As a result, these OEMs find they need to procure display modules based upon both the MDDI and MIPI™ standards. This places a burden on the manufacturer as it increases the number of display modules they must qualify and inventory, and reduces the scale of their volume purchasing power in securing favorable pricing for the display modules.

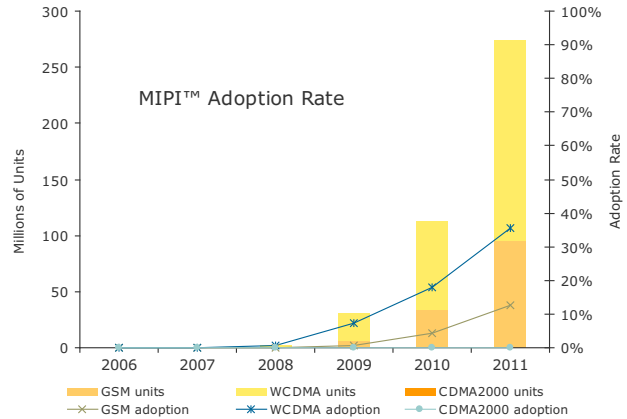
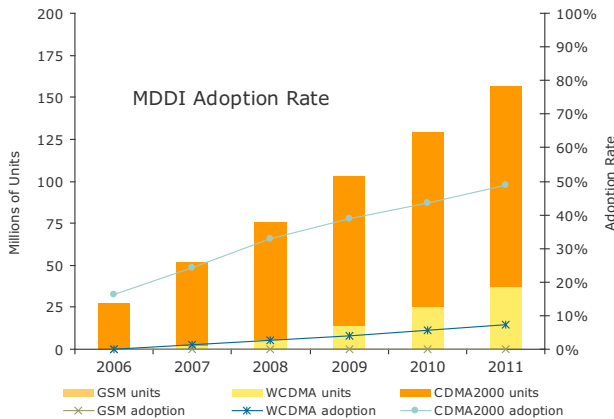


Figure 2. MDDI and MIPI™ Adoption Rates (Source: iSuppli Q4 2007)

An additional challenge faced by handset makers as they seek to deploy handsets based upon the new MIPI™ DSI standard is the potential for compatibility issues between CPU providers' MIPI™ host interfaces and MIPI™ client interfaces integrated into LCD display modules. The benefits of a compact four wire interface, reduced EMI emissions and lower power are attractive for a broad portfolio of feature phones and smart phones with display resolutions from QVGA through WVGA. Unfortunately, based upon the leadtime of getting new products based upon the MIPI™ standard to market, MIPI™ based CPUs will be available for a smaller set of price performance and feature segments during the first year of its introduction. This limits the number of handsets models in an OEM's portfolio that can take quickly take advantage of the benefits of a serial display interface.

A second concern is related to compatibility between the new MIPI™ DSI hosts and the MIPI™ DSI clients. A number of designs were started prior to the final completion of the standard. Additionally, differing interpretations of the specification by different MIPI™ host and client solution providers may lead to early compatibility issues. OEMs and solutions providers will have to devote additional resources to test and ensure compatibility of hosts and clients during the early adoption phase.

An Optimal Solution

What if a device existed that would enable a handset OEM to use any mobile CPU that features a legacy CPU interface, or MDDI client with LCD display modules based upon the MIPI™ DSI standard? Handset OEMs could take advantage of the benefits of a serial interface display standard while utilizing CPUs from multiple vendors, with or without MIPI™ or MDDI hosts, and leverage their purchasing volumes on display modules based upon a single standard. Furthermore, with a common MIPI™ host architecture, system level compatibility issues would be significantly reduced.

California Micro Devices has addressed this issue by introducing a device that can tie a variety of host interfaces to client

display devices using a single chip solution. The CM5160 MDDI-to-MIPI™ Interface Conversion IC and Serial Interface Bridge provides a unique solution to the display interface problem by allowing designers to "bridge" either MDDI or conventional CPU host interfaces to a serial display client based upon the MIPI™ standard.

CM5160 MDDI-to-MIPI™ Interface Conversion IC and Serial Interface Bridge: A Solution to Standards Adoption

A rich set of features enables a high level of design flexibility

The CM5160 MDDI-to-MIPI™ Interface Conversion IC and Serial Interface Bridge offers a unique solution for display interface implementation in handsets.

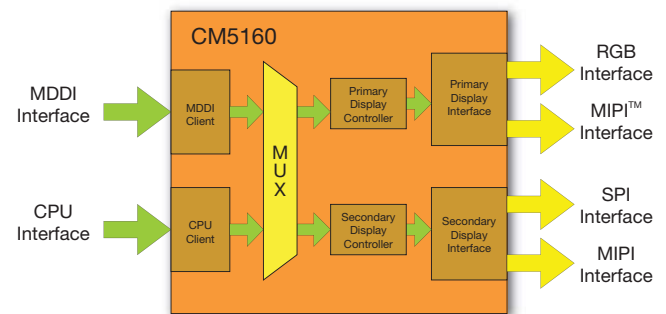


Figure 3. CM5160 Interfaces

As shown in Figure 3, the CM5160 bridges both MDDI and CPU host interfaces with either MIPI™ or traditional RGB clients, including smart panels. By providing support for both parallel CPU and standards-based serial interfaces, the CM5160 provides a flexible solution for implementing display interfaces, giving the handset designer the ability to mix and

match a number of existing host solutions with either a MIPI™ based or RGB client.

General Feature Set

Host Interfaces

The CM5160 provides two host interfaces to communicate with a host processor. The MDDI interface enables connection to a QUALCOMM MDDI host interface generally available on QUALCOMM's Mobile Station Modem™ (MSM™) processors. This interface accepts both a register and video packets from the host processor. The CPU client interface provides for those chipsets lacking a MDDI interface and consists of a standard I/O port with latch and chip select inputs.

MDDI Client Interface

The CM5160 provides a MDDI Type 1 client that interfaces to a host chipset supporting MDDI interface. The interface consists of a data and strobe interface, both using a differential LVDS scheme.

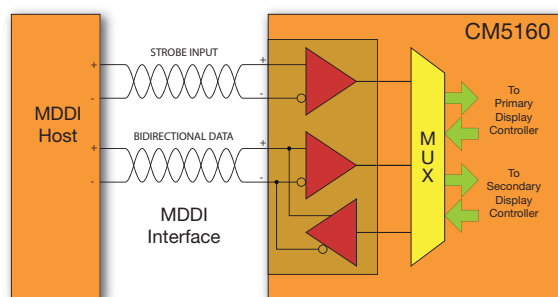


Figure 4. Simplified MDDI Interface Example

The data and clocking streams from the host are fed through de-serializing and packet parsing logic, resulting in either Register Access packets or Video Packets being forwarded on to the primary and secondary display controllers.

The MDDI client is also responsible for encapsulating input data from the display controllers and sending it back to the host.

The CM5160's MDDI client is VESA Version 1.0 Type 1 compliant and operates at up to 400Mbps. The following data packets and packet modes are supported:

- Sub-frame Header Packets
- Filler Packets
- Register Access Packets
- Round Trip Delay Measurement
- Reverse Link Encapsulation
 - + Client Capability
 - + Client Request and Status
 - + Client Return Register Read Data
- Forward Video
- Link Shutdown

The interface supports client wake-up from the primary display VSYNC or external GPIO inputs. The CM5160 MDDI Client interface supports 16, 18 or 24 bit video packets.

CPU Client Interface

For those host implementations that lack MIPI™ support, the CM5160 offers a generic CPU client interface enabling existing GSM and WCDMA CPUs to communicate with MIPI™ based LCD displays.

This client port supports 8, 9, 16, and 18 bit data transfers via a configurable 8, 9, 16, and 18 bit wide bus. The CPU client has its own register set to access internal registers and FIFOs. The CM5160 CPU interface supports 8, 16, 18 and 24 bit pixel data formats.

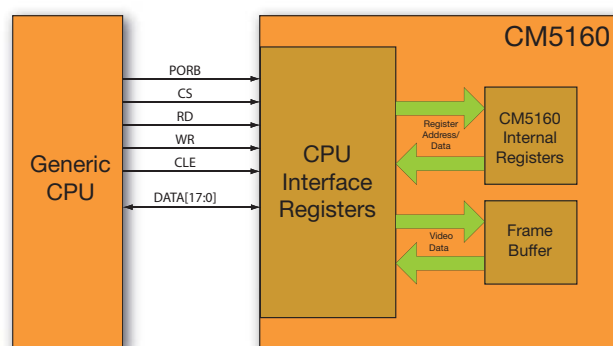


Figure 5. CPU Interface Block Diagram

Display Interfaces

The CM5160 features two display interfaces: 1) a primary display interface supporting RAM-less LCD modules, and 2) a secondary interface supporting Smart Panel LCD displays.

Primary Display Interface

The Primary Display Interface (PDI) embodies three key blocks: a frame buffer, a shadow register poller and a time controller (TCON). The primary display interface features two display output types: a DPI/RGB interface with standard VSYNC and HSYNC timing control outputs and a MIPI™ DSI Master interface. Both interfaces support either RAM-less or frame-buffer enabled LCD displays, including MIPI™ Type-1 (frame buffer enabled) and MIPI™ Type-4 (RAM-less) displays.

Embedded WQVGA Frame Buffer (423px by 240px by 24 bits)

The frame buffer is used to store incoming pixel data from the MDDI or CPU client interface. An onboard frame buffer facilitates the optional use of lower-cost RAM-less LCD modules on either interface, reducing handset display costs. The frame buffer can also be placed in pass-through (FIFO) mode in situations where a frame buffer is not needed, as in the case with MIPI™ Type-1 (frame buffer enabled) LCDs.

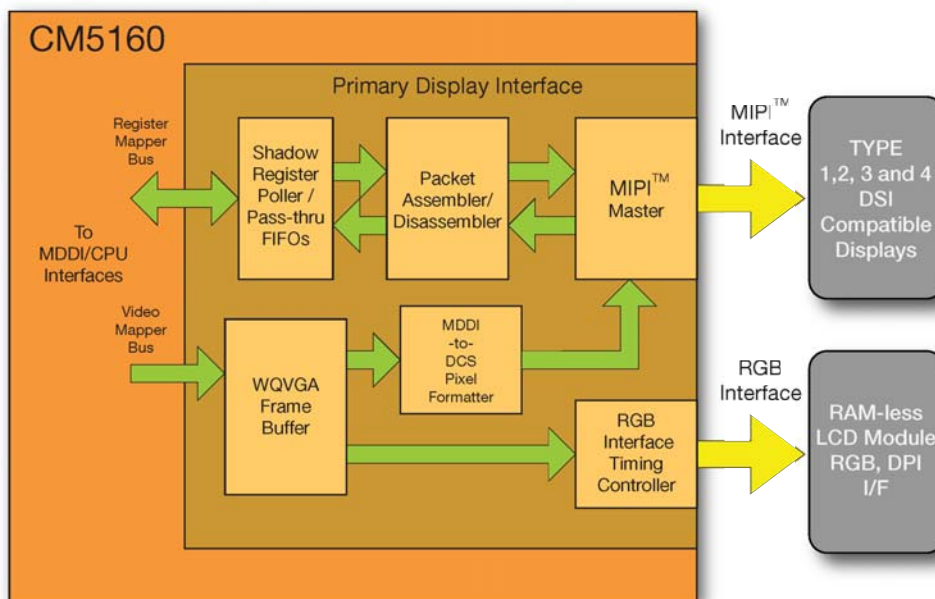


Figure 6. Simplified Block Diagram of the Primary Display Interface

MIPITM compatible Display Serial Interface (DSI/DCS)

The Primary Display Interface features a Master Display Serial Interface (DSI/DCS) for interfacing to MIPITM Type 1, 2, 3 and 4 DSI-compatible displays. This interface features either 1 or 2 data lanes with data rates up to 500Mbps per lane. This interface is designed to meet the MIPITM DSI specification version 1.01.00 R11 / D-PHY version 0.90.00. This interface operates in video mode only, command mode only or video mode with control mode packets transmitted during blanking intervals.

Video Mode

In video mode, packet transfers can be made with burst (time-compressed) and non-burst (real time) transfer modes. In non-burst mode, packets are sent with either sync pulses or sync events in the packet stream depending on whether or not real-time video synchronization timing is required. When real time sync is required, regular sync pulses are sent along with Sync Start Packets and Sync End Packets. When real-time video sync is not required, sync events are sent as Sync Start Packets along with the video packets.

In burst mode, RGB packets are time-compressed for non-real-time transfer, which facilitates the use of low-power mode or multiplexing other transmissions on the DSI link during the non-video interval.

Video mode supports 16-bit (5-6-5 packed format), 18-bit (6-6-6 packed / 6-6-6 loosely packed formats) or 24-bit (8-8-8 packed format) pixel streams.

Command Mode

Command mode facilitates the transfer of control packets to and from the display module, where applicable. Control packets are passed to and from the display via the MIPITM Master Forward Link and Reverse Link ports. Data to be encapsulated as outbound control packets are queued to this port in the Shadow Register Poller and transfer is managed independently, freeing the host processor from having to manage the control packet forwarding process. Control packets received at the Reverse Link port are placed in the receiving Shadow Register FIFO where the CPU or MDDI host can retrieve read responses when it has bandwidth available.

RGB / Display Parallel Port Interface

For displays lacking MIPITM DSI support, the CM5160 features a full 24-bit RGB parallel port interface supporting 16, 18 and 24-bit output formats. In conjunction with the CM5160's on-board frame buffer, this interface supports lower-cost RAM-less LCD panels.

Standard vertical (VSYNC) and horizontal sync (HSYNC) outputs are provided. It also incorporates an automatic anti-tear prevention feature, improving display appearance. The interface supports frame refresh rates up to 100Hz.

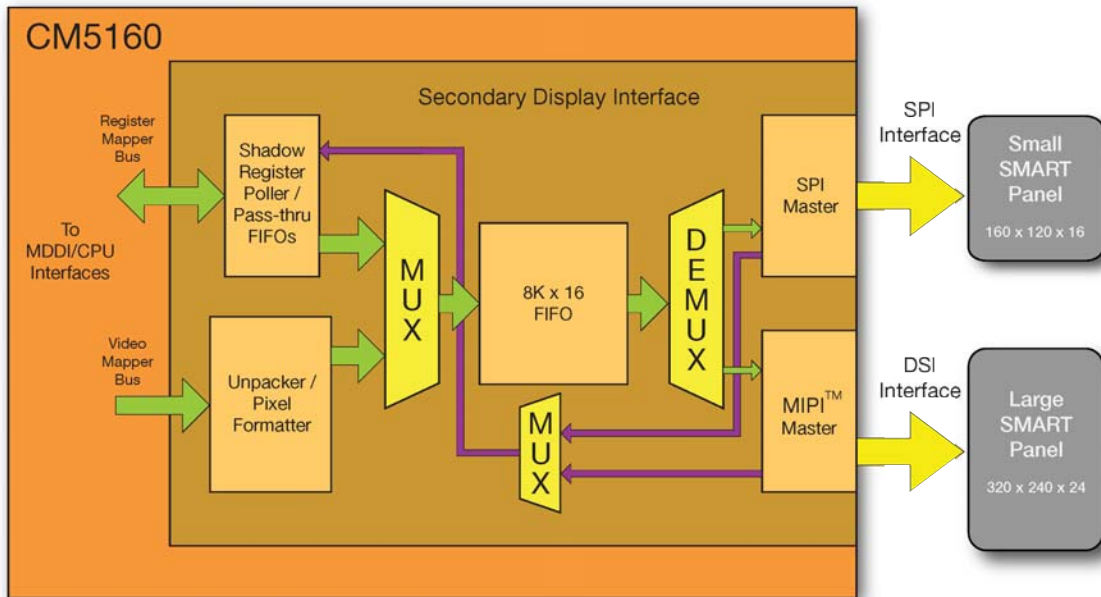


Figure 7. Simplified Block Diagram of the Secondary Display Interface

Secondary Display Interface

The CM5160 Secondary Display Interface (SDI) features a SPI/DBI-C interface and a MIPI™ DSI interface, both suitable for interfacing with SMART panels. The SDI has its own native Shadow Register Poller / FIFO for packet transfer to and from the SDI.

The Secondary Display Interface is designed to support driving a QVGA or higher resolution display.

Serial Peripheral Interface (SPI) / DBI-C Interface

The Serial Peripheral Interface features a 3/4 wire serial interface. This interface features a programmable clock frequency, which is derived from the onboard PLL block. The SPI interface features two select outputs which facilitate using one of the SPI interfaces for primary display setup and the other for a secondary display module.

MIPI™ Display Serial Interface (DCS)

The Secondary Display Interface features a Master MIPI™ Display Serial Interface (DSI) consisting of a single data lane with up to 500Mbps transfer rate. The DSI is compliant to MIPI™ DSI Version 1.01.00 R11 and is Version 0.90.00 D_PHY physical layer compliant. This interface operates only in command mode.

Other Features

Low Drop Out (LDO) Regulator

The CM5160 provides an onboard LDO regulator which supplies 1.5V for the chip's core, eliminating the need for a separate supply to be generated.

Embedded Phase Locked Loop Reference Multiplier

The CM5160 provides an onboard Phase Locked Loop / Reference Multiplier that is used to provide timing for internal logic and register operations as well as clock reference for the MIPI™ DSI and SPI interfaces.

The PLL can be bypassed when an existing external reference clock is available, thus saving power when the PLL operation is disabled.

Power Management

Several power management modes are available on CM5160 to conserve power when the interfaces are not active. Besides turning off clocks in the function blocks that are not active, or turning off unused MDDI /MIPI™ transceivers, one external input pin "CHIP_SHUTDOWN" can place the entire chip under sleep mode. Under sleep mode, the chip consumes very minimum power, and maximum power saving can be achieved. The following table summarizes several power management modes.

POWER MANAGEMENT MODE SUMMARY						
MODE	CHIP SHUT-DOWN PIN	PLL POWER DOWN	MEMORY POWER ON	MDDI DATA DRIVER PDN	MDDI MAIN BIAS POWER DOWN	MODE DESCRIPTION AND TYPICAL FUNCTION
	B8103, BIT 0	B8106, BIT 0	B8107, BIT 0	B8304, BIT 0	B8103, BIT 0	
SLEEP	0	X	X	X	X	Config Reg settings are retained. SRAM contents are lost. All functions disabled.
HIBERNATE (HBR-1)	1	1	1	0	1	Config Reg settings are retained. SRAM contents are lost and non-writable. MDDI Link is waiting for wakeup.
HIBERNATE (HBR-2)	1	1	0	0	1	Config Reg settings are retained. SRAM contents are retained. MDDI Link is waiting for wakeup.
HIBERNATE (HBR-3)	1	0	0	0	1	Config Reg settings are retained. SRAM contents are retained. MDDI Link is waiting for wakeup. Clocks and PD refresh enabled.
LINK ACTIVE (LNK_ACT-RO)	1	0	0	0	1	Config Reg settings are writable. SRAM contents are writable. MDDI Link is active, receiving data. Video and audio streaming enabled.
LINK ACTIVE (LNK_ACT-BD)	1	0	0	1	1	Config Reg settings are readable/writable. SRAM contents are readable/writable. MDDI Link is active, receiving and transmitting data. Streaming with read back enabled.

Conclusion

The existence of two industry standards for high speed serial display interfaces has forced handset manufacturers to manage inventory for various LCD modules dependent upon the specific serial interface standard supported by their CPU selection. With the availability of the new CM5160 MDDI-to-MIPI™ bridge, handset manufacturers utilizing a CPU with an MDDI based host will have the flexibility to procure display modules with either an MDDI based client or a MIPI™ based client. Handset manufacturers that produce systems based on both the GSM and CDMA standards and associated 3G standards, will have the opportunity to achieve cost savings as a result of focusing their volume purchasing power on LCD modules based on a single standard while realizing cost, space, power and EMI reduction advantages of a serial interface.

In addition to providing multi-standard display module support for MDDI based CPU handsets, the new CM5160 MDDI-to-

MIPI™ bridge can also interface to existing GSM and WCDMA baseband CPUs and application processors via an industry standard CPU interface. This will enable handset manufacturers seeking an early introduction of MIPI™ based handset designs the additional flexibility of utilizing widely available GSM and WCDMA CPUs that do not feature an integrated MIPI™ host. Handset manufacturers can reduce product launch risks associated with dependence upon new product development schedules while taking full advantage of the benefits of a high speed serial display interface.

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